AMENDMENTS TO THE SPECIFICATION

Please delete the sixth paragraph on page 4 and replace it with the following amended paragraph:

figures 1A-1F ~~is a~~are schematic diagrams of one embodiment of the invention that allows definition of source and drain electrode of a planar FET with high resolution.

Please delete the eighth paragraph on page 4 and replace it with the following amended paragraph:

figures 3A-3B ~~is a~~are schematic diagrams of a top-gate planar FET device with a gate electrode that is self-aligned with the source and drain electrodes.

Please delete the first paragraph on page 5 and replace it with the following amended paragraph:

figures 4A-4C ~~is a~~are schematic diagrams of a bottom gate planar FET device with a gate electrode that is self-aligned with the source and drain electrodes.

Please delete the third paragraph on page 5 and replace it with the following amended paragraph:

figures 6A-6C shows ~~a~~ device structures for a vertical-channel FET with a selfaligned gate electrode.

Please delete the fourth paragraph on page 5 and replace it with the following amended paragraph:

figures 7A-7C shows another device structure for a vertical-channel FET with a self-aligned gate electrode.

Please delete the fifth paragraph on page 5 and replace it with the following amended paragraph:

figures 8A-8C shows a process for defining a surface energy pattern by embossing.

Please delete the sixth paragraph on page 5 and replace it with the following amended paragraph:

figures 9A-9D shows another process for defining a surface energy pattern by embossing.

Please delete the seventh paragraph on page 5 and replace it with the following amended paragraph:

figures 10A-10C shows various processes for locally increasing the capacitance of a dielectric layer.